A Flexible 10-300 MHz Receiver IC Employing A Bandpass Sigma-Delta ADC

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***Abstract* — This 0.6 μm BiCMOS IC mixes a 10-300 MHz first IF down to a 1.5-3 MHz second IF and digitizes the result with a bandpass sigma-delta ADC. The ADC achieves 88 dB SNR in a 10 kHz bandwidth, 75 dB SNR in a 200 kHz bandwidth and >90 dB of image rejection while consuming only 8 mA from a 2.7 V supply. The complete IC, which incorporates an LNA, mixer, active anti-alias filter, VGA, ADC, decimation filter and two synthesizers, achieves a noise figure of 11 dB and an IIP3 of -1 dBm with a power consumption of 120 mW.**

I. Introduction

RF communication systems differ in modulation format, frequency assignment and access protocol, but have in common the need for receivers with high dynamic range and low power consumption. Digital signal processing of the received signal before conversion to audio mandates the use of an analog-to-digital converter (ADC) within the receiver. The location of the ADC within the signal chain presents the receiver designer with a number of options.

The ADC may be placed after a complex mix to baseband or it may digitize one of the intermediate frequencies within the receiver. A baseband ADC can be made very power-efficient (Breems et al. achieve 86 dB dynamic range with BW = 100 kHz and P = 1.8 mW [1]), but the receiver architecture suffers from imperfect I/Q balance due to the use of analog mixing and separate I/Q ADCs. Digitizing an IF avoids the aforementioned problems associated with baseband conversion but requires the use of a high-speed higher-power ADC. Since the ADC's input is narrowband, it is inefficient to require the ADC to accurately digitize all frequencies from dc to half the sampling rate, only to have most of these frequencies removed by subsequent filtering. A more elegant approach involves the use of an ADC which accurately digitizes only those frequencies within the desired band. A bandpass sigma-delta ADC fits this description precisely.

Fig. 1 illustrates a bandpass sigma-delta ADC in which the difference between the input signal and the fed-back digital output is passed through an analog filter possessing high (ideally infinite) gain at the center of the band-of-interest; the output of the filter is quantized coarsely (often to only a single bit) to form the digital output [2-4]. Like lowpass sigma-delta ADCs, bandpass sigma-delta ADCs possess noise-shaped output spectra and can achieve very high dynamic range. The main distinction between the two converter types is that the null in the quantization noise is located at DC for a lowpass converter but at the IF frequency for a bandpass converter.

In this paper, a receiver IC which incorporates a bandpass sigma-delta ADC is described. Architectural tradeoffs are presented first, followed by specifications and later measurements of two key blocks.

II. Architectural Choices

As shown in Fig. 2, the IC incorporates many blocks associated with the second half of a dual-conversion superheterodyne receiver. The signal chain consists of a low-noise amplifier (LNA), a mixer, a variable-gain amplifier/anti-alias filter block, a bandpass sigma-delta ADC and a digital decimation filter. On-chip automatic gain control (AGC) logic ensures full use of the ADC's dynamic range. Also included on the IC are two synthesizers, one for the second LO and one for the ADC's sampling clock, plus digital interface and control circuitry. The first and second image-reject filters, the first down-conversion mixer and the voltage-controlled oscillators are off-chip, as is the digital signal processor (DSP).

To allow the IC to be used in a variety of applications, the range of the first IF is quite large (10 to 300 MHz) and many of the system parameters are programmable. For example, the decimation factor of the digital decimation filters is variable from 60 to 960 (supporting output data rates from 400 kHz to 25 kHz at f_{CLK} = 24 MHz); the AGC bandwidth is variable from 70 Hz to 12 kHz (f_{CLK} = 24 MHz); and the ADC clock frequency spans 12 to 24 MHz.

To support a broad range of input frequencies while

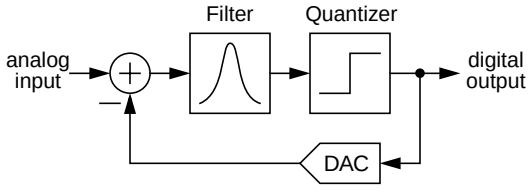

Fig. 1: Structure of a bandpass sigma-delta ADC.

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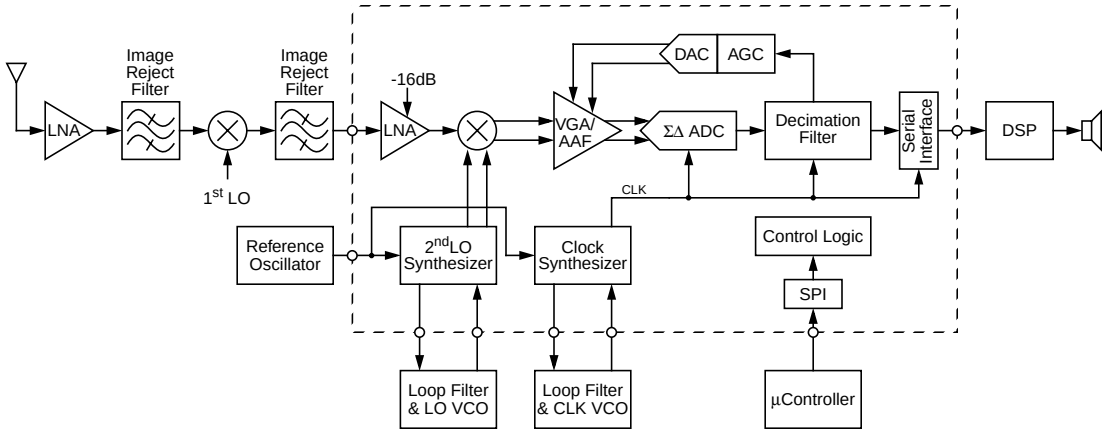

Fig. 2: Simplified receiver block diagram, showing the blocks internal to and peripheral to the IC.

minimizing the number of external components, frequency-selective elements are not used in the on-chip LNA or mixer. For similar reasons, there is no image-reject filter between the LNA and the mixer. The drawback of these topology choices is that amplified image noise at the output of the LNA is downconverted along with the desired signal to the second IF, increasing the 3 dB noise figure of the LNA/Mixer by $20\log(2/\pi) = 3.9$ dB. An architecture in which an analog quadrature mix is followed by complex A-to-D conversion [5] eliminates much of the image noise, but nearly doubles the area and power of the analog circuitry.

A second architectural choice revolves around the location of the boundary between continuous-time signals and discrete-time signals. If the ADC is constructed from continuous-time elements, precise tuning of those elements is required to realize accurate quantization noise nulls. However, if the ADC uses a switched-capacitor filter, the placement of the noise nulls can be very precise because the filter's characteristics are determined by capacitor ratios. This fact, combined with the fact that an ADC implemented with switched-C technology requires no off-chip components, makes a switched-C ADC an attractive architectural choice.

Ideally, the dynamic range of the ADC would be large enough to digitize the full output range of the mixer, without resorting to variable gain elements. With a target system dynamic range in excess of 90 dB, this goal appears reasonable at first glance. However, to minimize the impact of ADC noise on the system noise figure, the dynamic range of the ADC must be 10-15 dB greater than the desired system dynamic range. This more demanding dynamic range requirement makes an AGC-free system consume more power than one which incorporates a variable-gain amplifier (VGA). Since the ADC must be preceded by an anti-alias filter anyway, it is power-efficient to combine the anti-alias and variable-gain functions in a single block.

The anti-alias requirements are determined by the selectivity of the external image-reject filter and the spacing between the ADC's passband and the first alias. A common choice for the center frequency (f_0) of a bandpass ADC is $f_{CLK}/4$, since this choice makes digital downconversion trivial. However, this choice only provides approximately 1.5 octaves between the center of the ADC's passband at f_0 and the first alias at $3f_0$. If $f_0 = f_{CLK}/8$ instead, the first alias is at $7f_0$, providing 2.8 octaves of separation and thereby easing the design of the AAF. Fortunately, by exploiting the technique outlined in [6], the increase in the complexity of the digital downconversion/decimation is small.

The on-chip synthesizers allow the IC to synthesize the second LO and the ADC sampling clock. The maximum LO frequency of 300 MHz is limited by the achievable LNA bandwidth. The ADC clock frequency is determined by balancing the need for a high clock frequency to maximize the benefits of noise-shaping with the desire to minimize the clock frequency to minimize power consumption. To allow flexibility in frequency planning, the ADC clock frequency is allowed to span a 2:1 range from 12 MHz to 24 MHz. The loop filters and the VCOs are external since they can then take advantage of discrete L and C elements to achieve low phase noise with the least possible power consumption.

III. Block Specifications and Performance

To achieve a low noise figure while keeping the power consumption low, the input impedance of the LNA should be high. However, a high input impedance results in large voltage swings for a given input power and hence degrades linearity. With a 300 ohm input impedance and an input

power of -20 dBm, the input to the LNA is approximately 0.15 V_{pp}. Allowing a voltage gain of 15 dB (5.6 V/V) for the LNA, the output of the LNA swings 0.9 V_{pp}, which is approximately the largest signal that can be supported with a simple common-emitter amplifier powered from 2.7 V. To trade linearity for reduced power consumption, the LNA bias current can be programmed to one of 4 values from 0.5 to 3 mA. Since the LNA is a simple resistively-degenerated common-emitter amplifier, the load resistance is programmed via MOS switches in conjunction with the bias current to maintain 15 dB of gain.

The double-balanced mixer uses a multi-tanh V-I converter [7] attached to a Gilbert mixing core, and drives on-chip resistive loads. A programmable capacitor across the mixer outputs implements one pole of the AAF. The capacitor is programmable to account for the 2:1 range of f_{CLK} and the ±40% variation of on-chip time-constants. The mixer pole is positioned at approximately $2f_0$ to minimize attenuation of the signal at f_0 and the resulting increase in system noise figure.

The remainder of the AAF is built around the variable gain amplifier (VGA). Fig. 3 shows how the anti-alias function is distributed along the signal chain. The filter is essentially third-order (a fourth pole above 80 MHz provides extra attenuation beyond 100 MHz) and is made tunable by implementing C_0-C_2 with capacitor arrays. Tuning is accomplished by measuring the oscillation frequency of an on-chip RC reference oscillator against f_{CLK}. Since this measurement is ratiometric, the anti-alias response tracks the clock frequency and provides alias protection that scales with f_{CLK}. Fig. 4 shows the measured response of the AAF. The first alias is at $(7/8)f_{CLK}$ = 21 MHz and the filter provides more than 30 dB of attenuation at this alias. The filter displays the expected 60 dB/decade roll-off and more than 65 dB of attenuation for frequencies above 100 MHz.

The VGA gain is adjustable from 10 to 32 dB. The VGA contains a linearized V-I converter connected to a multiplier and then to an op-amp for I-V conversion. The VGA, the LNA and the mixer are the primary users of the 25 GHz bipolar transistors available in the 0.6 µm BiCMOS process. The continuously-variable gain and on-chip AGC allows use of the IC in a fast-fading environment.

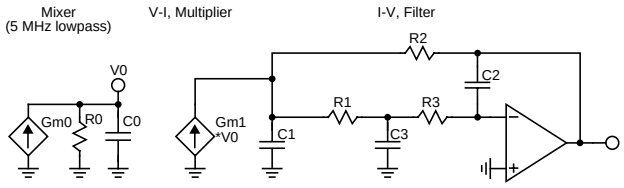

Fig. 3: Small-signal, single-ended equivalent of the AAF.

To achieve a high dynamic range with a minimum of power, the bandpass sigma-delta ADC makes use of multi-bit quantization. As shown in Fig. 5, the ADC is a fourth-order modulator containing two switched-capacitor resonators and a 9-level quantizer. A digitally-implemented $1+z^{-4}$ mismatch-shaping transfer function [8] attenuates the in-band errors caused by element mismatch. Fig. 6 shows the measured spectrum of the ADC's output before decimation, superimposed on the predicted quantization noise density. Fig. 7 shows the complex spectrum of the decimated output with a 2-tone input to the VGA. Intermodulation products, image spurs and DC offset are all less than -100 dB relative to full-scale.

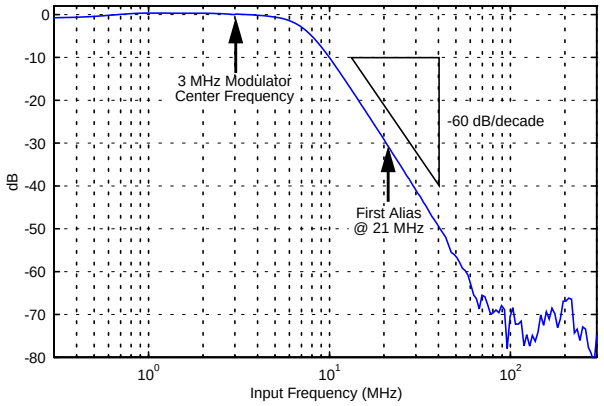

Fig. 4: AAF response after tuning. f_{CLK} = 24 MHz.

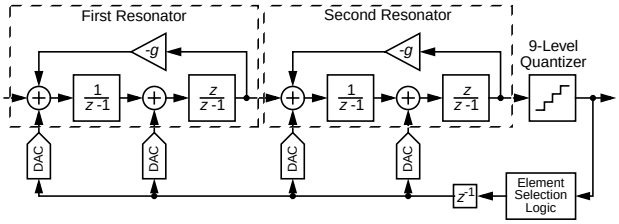

Fig. 5: ADC Block Diagram.

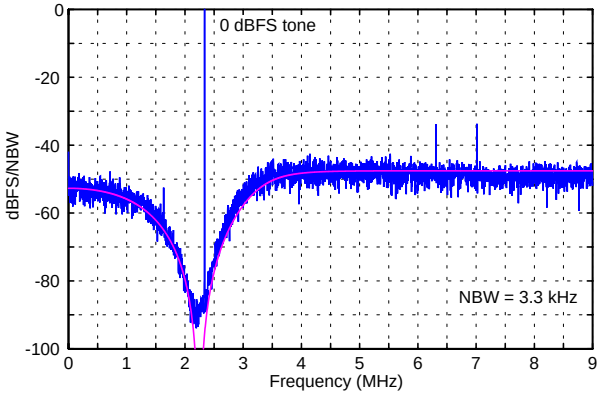

Fig. 6: Undecimated modulator output spectrum. (ADC in isolation, f_{CLK} = 18 MHz.)

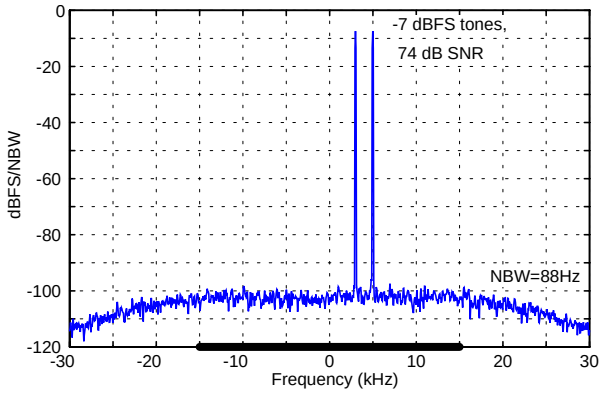

Fig. 7: Decimated complex output spectrum.
(VGA at max. gain, f_{CLK} = 18 MHz, BW=30 kHz.)

The decimation filter is programmable for decimation factors from 60 to 960 and provides 88 dB of alias protection. Dynamic logic is used to minimize both the area and the power consumed by the filter.

IV. System Performance

Table 1 summarizes the IC's performance. For a signal bandwidth of 10 kHz, the total system dynamic range is 91 dB with 120 mW power consumption. Programming the IC for minimum power consumption saves 25 mW without causing an increase in system noise figure, but does degrades the IIP3 from -1 dBm to -22 dBm.

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References

[1] L. Breems et al., "A 1.8 mW CMOS ΣΔ modulator with integrated mixer for A/D conversion of IF signals," *IEEE Journal of Solid-State Circuits*, vol. SC-35, pp. 468-475, April 2000.

[2] T. H. Pearce and A. C. Baker, "Analogue to digital conversion requirements for HF radio receivers," *Proceedings of the IEE Colloquium on system aspects and applications of ADCs for radar, sonar and communications*, London, Nov. 1987, Digest No 1987/92.

[3] P. H. Gailus, W. J. Turney, F. R. Yester Jr., "Method and Arrangement for a Sigma Delta Converter for Bandpass Signals," U.S. Patent no. 4,857,928, filed Jan. 28 1988, issued Aug. 15 1989.

[4] R. Schreier and W. M. Snelgrove, "Bandpass Sigma-Delta Modulation," *Electronics Letters*, vol. 25, no. 23, pp. 1560-1561, 9th Nov. 1989.

[5] T. Paulus et al., "A CMOS IF transceiver with reduced analog complexity," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 2154-2159, Dec. 1998.

[6] R. Schreier and W. M. Snelgrove, "Decimation for bandpass sigma-delta analog-to-digital conversion," *Proceedings of the 1990 IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 1801-1804, May 1990.

[7] B. Gilbert, "The multi-tanh principle: a tutorial overview," *IEEE Journal of Solid-State Circuits*, vol. SC-33, pp. 2-17, Jan. 1998

[8] T. Shui and R. Schreier, "Mismatch shaping for a current-mode multibit delta-sigma DAC," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 331-338, March 1999.

[9] E. van der Zwan et al., "A 10.7 MHz IF-to-baseband ΣΔ A/D conversion system for AM/FM radio receivers," *ISSCC Digest of Technical Papers*, pp. 340-341, Feb. 2000.

[10] A. Tabatabaei, K. Kaviani and B. Wooley, "A two-path bandpass ΣΔ modulator with extended noise shaping," *ISSCC Digest of Technical Papers*, pp. 342-343, Feb. 2000.

[11] H. Tao and J. Khoury, "A 100MHz IF, 400 MSample/s CMOS direct-conversion bandpass ΣΔ modulator," *IEEE Journal of Solid-State Circuits*, vol. SC-34, pp. 1741-1752, Dec. 1999.

[12] J. van Engelen et al., "A 6th-order continuous-time bandpass ΣΔ modulator for digital radio IF," *IEEE Journal of Solid-State Circuits*, vol. SC-34, pp. 1753-1764, Dec. 1999.

[13] T. Paulus et al., "A CMOS IF transceiver with reduced analog complexity," *IEEE Journal of Solid-State Circuits*, vol. SC-33, pp. 2154-2159, Dec. 1998.

Parameter	Value	Notes
Input Frequency	10-300 MHz	
Power consumption @ 2.7 V	120 mW	Full power configuration
	95 mW	Min. power configuration
VGA gain range	22 dB	
ADC clock rate	12-24 MHz	
ADC center frequency	$f_{CLK}/8$	
ADC bandwidth	6.25-200 kHz	
ADC signal-to-noise ratio	88 dB	BW = 10 kHz
	75 dB	BW = 200 kHz
System Sensitivity	-113 dBm	8 dB SNR at BW=10kHz
Full-Scale Input Level	-44 dBm	VGA at max gain
	-22 dBm	VGA at min gain
System Dynamic Range	91 dB	(Max. F.S.) - (Sensitivity)
Input Impedance	300 ohm	
System Noise Figure	11 dB	
Input IP3	-1 dBm	Full power configuration.
	-22 dBm	Min. power configuration

Table 1: Performance Data